CLAIMS:

1. A circuit arrangement, particularly for a television, multimedia, radio or video recording device, for transition from a range of low voltage (U_i) to a range of high voltage (U_o), characterized in that at least one adapter circuit (10) is provided, which amplifies a particularly analog input signal of a low current (I_i) by an amplification factor (n) into a particularly analog output signal of a higher current (I_o),

- whose input (12) is assignable to the range of low voltage (U_i),
- whose output (18) is assignable to the range of higher voltage (U_o), and
- comprises at least one npn transistor current mirror (14) and
- at least one pnp current mirror (16) arranged in series with the npn transistor current mirror (14) and connected to at least one high voltage source (30).

2. A circuit arrangement as claimed in claim 1, characterized in that the amplification factor (n) is approximately 5.

3. A circuit arrangement as claimed in claim 1 or 2, characterized in that the signal is amplified in the pnp current mirror (16) or in the npn transistor current mirror (14).

4. A circuit arrangement as claimed in any one of claims 1 to 3, characterized in that the high voltage source (30) supplies a voltage of the order of approximately 12 V.

5. A circuit arrangement as claimed in any one of claims 1 to 4, characterized in that the input (12) of the adapter circuit (10) is preceded by at least one supply or driver circuit (40) by which the low current (I_i) input signal can be applied to the adapter circuit (10).

6. A circuit arrangement as claimed in claim 5, characterized in that the supply or driver circuit (40) is connected to at least one low voltage source (42).

7. A circuit arrangement as claimed in claim 6, characterized in that the low voltage source (42) supplies a voltage of the order of approximately 1 V to approximately 3.3 V.

8. A circuit arrangement as claimed in any one of claims 1 to 7, characterized in that

- the npn transistor arrangement (14) is constituted as an npn current mirror and/or particularly as an NMOS current mirror (NMOS = N-channel Metal Oxide Semiconductor = N-type Metal Oxide Semiconductor); and/or
- the pnp transistor arrangement (16) is constituted as a pnp current mirror and/or particularly as a PMOS current mirror (PMOS = P-channel Metal Oxide Semiconductor = P-type Metal Oxide Semiconductor).

9. A circuit arrangement as claimed in any one of claims 1 to 8, characterized in that the output (18) of the adapter circuit (10) precedes at least a resistor (50) for converting the higher current (I_o) output signal into a higher voltage (U_o) output signal.

10. A circuit arrangement as claimed in claim 9, characterized in that the resistor (50) has a value of approximately 1 kΩ.

11. A circuit arrangement as claimed in any one of claims 1 to 10, characterized in that the output (18) of the adapter circuit (10) precedes at least a SCART (= Syndicat des Constructeurs d'Appareils Radio Receteurs et Televiseurs) output (70).

12. A circuit arrangement as claimed in any one of claims 1 to 11, characterized in that the adapter circuit (10) is multi-staged and/or more than one adapter circuit (10) is provided.

13. A circuit arrangement as claimed in claim 12, characterized in that eight npn transistors (14) and 24 pnp transistors (16) are provided, and in that the four-stage adapter circuit (10) or the four adapter stages (10) precede a resistor (50).

14. A television, multimedia, radio or video recording device comprising at least a circuit arrangement (100) as claimed in any one of claims 1 to 13.